



Adesto

eXecute-in-Place for Low-Power IoT and Instant-on Smart Devices (Preview)

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Short history of NVM in embedded systems

- In the beginning...
 - Byte-wide ROM and EPROM were used as the Non-Volatile Memory in most embedded systems
 - Parallel NOR Flash devices were introduced in the late 80s and gradually replaced their predecessors
- Typical use case was eXecute-in-Place (XiP)
 - Though, that term did not exist at that time
 - Four byte-wide Flash devices typically created a 32-bit wide bus for the CPU
 - Latency and throughput delivered by the Flash array were sufficient for the fastest CPUs of that era



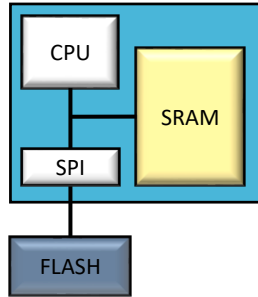
Faster PCs changed the picture

- The speed of CPUs ramped up beyond 1GHz
 - While NOR Flash devices could not keep up with these frequencies
 - XiP was abandoned and application code was now running from DRAM
 - NOR Flash was relegated to only support the system-boot operation
- In this new world, the speed of the Flash device was no longer important
 - Upon start-up, hardware would copy the contents of the Flash to DRAM and the Flash would not be needed until the next boot sequence
 - Atmel and later other suppliers came up with the Serial Flash
 - Smaller footprint and lower cost than parallel NORs
 - But, delivering much lower data throughput
 - Still, this was good enough for the new role of the Flash device

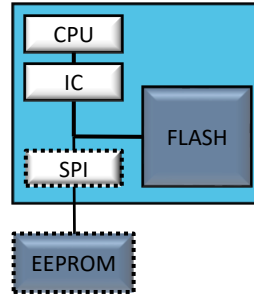


Today's IoT systems: one of three architectures

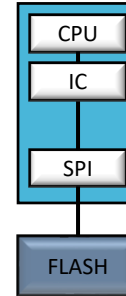
Shadow Flash, on-chip SRAM



Embedded NVM



XiP NVM



- **Shadow Flash:** Upon boot, the code is copied to and executed from an internal SRAM (or external DRAM)
- **Embedded NVM:** Flash device is part of the IoT SOC, code is executed directly out of it
- **XiP:** Code executed directly from an external NOR Flash

Combinations of these basic architectures are gaining momentum

The problem

- Class of devices requiring intelligent local data processing capability
 - Relatively large program memory
 - Higher performance time critical applications
- Embedded flash only addresses low- to mid-range products
 - Limited scalability
 - Limited memory
 - Higher cost SoCs as a result of more expensive and “shrink-resistant” silicon process
- External DRAMs address only the highest-end products
- Existing solutions are power-hungry, performance-limiting and expensive

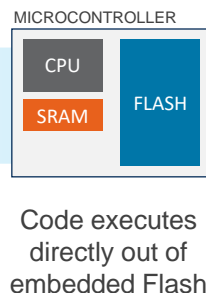
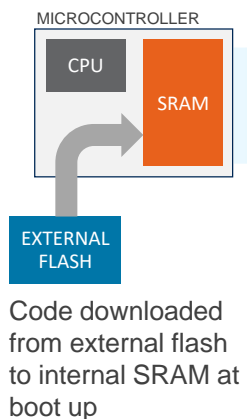
The need for eXecute-in-Place

microcontrollers removing / reducing embedded flash

YESTERDAY

Code Shadow

Embedded Flash



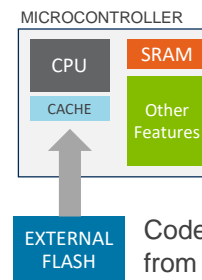
SMALLER
SILICON GEOMETRIES

Embedded flash
more expensive or unavailable

SRAM leakage current
becomes more significant

TODAY

eXecute-in-Place (XiP)



- Embedded flash removed or reduced
- SRAM optimized

- Lower solution cost
- Higher processing speeds
- SRAM power impact reduced
- “Instant On” capabilities

The solution

- An NVM device designed specifically for eXecute-in-Place
 - High enough bandwidth on the interface between the Flash and the SoC
 - Optimized to deliver performance in cached-based CPUs
 - Easy handling of Over-The-Air (OTA) updates
 - Low power consumption in fetch (read) operations
 - Power down modes to support down-times of the IoT device
- The rest of this presentation will show:
 - How to handle each of the above design targets
 - Adesto's EcoXiP family of NVM devices for XiP applications
 - Performance and power characteristics of the EcoXiP when operating with NXP's i.MX RT1050

**Attend the session to
learn more!**